Patent NASA Case No.: NPO-20535-2--CU

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IN THE CLAIMS

Please insert the following claims in place of the currently pending claims:

1. (Currently Amended) An evolvable circuit, comprising:

a plurality of transistors, each of said transistors comprising a first power terminal, a second power terminal and a control terminal;

a plurality of reconfigurable switches, each single one of said switches providing an individual interruptable terminal-to-terminal connection among said transistors, said plurality of reconfigurable switches comprising:

a first plurality of reconfigurable switches that when in a closed position ~~connected to~~ form a first series-connected succession of said transistors, whereby each pair of successive transistors in said succession have a connection at the first power terminal of one transistor and the second power terminal of the other transistor of the pair through a corresponding single reconfigurable switch, each connection being governed by the corresponding single reconfigurable switch.

2. (Original) The circuit of Claim 1 wherein the number of said transistors exceeds three and the number of said reconfigurable switches is within an order of magnitude of the number of terminals of said plurality of transistors, said number of terminals including said first power terminals, said second power terminals and said control terminals of said plurality of transistors.

3. (Original) The circuit of Claim 2, wherein said plurality of reconfigurable switches comprises reconfigurable switches having variable conductance states.

4. (Original) The evolvable circuit of Claim 1 wherein said plurality of reconfigurable switches further comprises:

PAGE 3/30 * RCVD AT 10/13/2006 1:03:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/19 * DNIS:2738300 * CSID:818 393 3160 * DURATION (mm-ss):11-28

a second plurality of reconfigurable switches connected between the first power terminals of respective pairs of said transistors.

5. (Original) The evolvable circuit of Claim 4 wherein said plurality of reconfigurable switches further comprises:

A third plurality of reconfigurable switches, each respective one of which is connected between the control terminal and said first power terminal of a respective one of said transistors.

6. (Original) The circuit of Claim 5 wherein said first plurality of reconfigurable switches forms plural respective series-connected successions of transistors that are parallel to one another, and wherein said plurality of reconfigurable switches further comprises:

a fourth plurality of reconfigurable switches each connected between the control terminals of a pair of corresponding ones of the transistors in different ones of said series-connected successions of transistors.

7. (Original) The circuit of Claim 6 wherein said plural series-connected successions of transistors are arranged in columns of transistors, the corresponding transistors in different columns forming rows of transistors, the transistors in a first plurality of said rows being of a first conductivity type and the transistors in the remaining ones of said rows being of a second conductivity type complementary to said first conductivity type.

8. (Original) The circuit of Claim 6 wherein said plurality of reconfigurable switches further comprises:

A fifth plurality of reconfigurable switches connected between one of said first and second power terminals of the transistors of different ones of said series-connected successions of transistors.

PAGE 4/30 * RCVD AT 10/13/2006 1:03:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/19 * DNIS:2738300 * CSID:818 393 3160 * DURATION (mm-ss):11-28

9. (Original) The circuit of Claim 8 wherein said plurality of reconfigurable switches further comprises:

a reconfigurable switch connected between the first power terminal of a transistor in one of said series-connected successions of transistors and the second power terminal of a transistor of a different one of said series-connected successions of transistors.

10. (Original) An evolvable circuit comprising:

a plurality of transistors, each of said transistors comprising a first power terminal, a second power terminal and a control terminal;

a plurality of reconfigurable switches, each single one of said reconfigurable switches providing an individual interrruptable terminal-to-terminal connection in said plurality of transistors; and

all terminal-to-terminal connections among said plurality of transistors being provided through respective ones of said plurality of reconfigurable switches with the exception of connections through voltage sources.

11. (Currently Amended) The circuit of Claim 10 wherein the plurality of transistors comprises at least one transistor cell comprising eight transistors in a two column by four row configuration ~~number of said reconfigurable switches is within an order of magnitude of the number of terminals of said plurality of transistors, said number of terminals including said first power terminals, said second power terminals and said control terminals of said plurality of transistors~~.

12. (Currently Amended) The circuit of Claim 11, comprising a plurality of cells connected by at least one pair of transistors ~~wherein the number of said reconfigurable switches is at least nearly the same as the number of terminals of said plurality of transistors~~.

PAGE 5/30 * RCVD AT 10/13/2006 1:03:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/19 * DNIS:2738300 * CSID:818 393 3160 * DURATION (mm-ss):11-28

13. (Original) An evolvable circuit comprising:

a plurality of transistors, each of said transistors comprising a first power terminal, a second power terminal and a control terminal;

a plurality of reconfigurable switches, each single one of said reconfigurable switches providing an individual interruptable terminal-to-terminal connection in said plurality of transistors; and

wherein the number of said reconfigurable switches exceeds three and the number of said reconfigurable switches is within an order of magnitude of the number of terminals of said plurality of transistors, said number of terminals including said first power terminals, said second power terminals and said control terminals of said plurality of transistors.

14. (Currently Amended) The circuit of Claim 13, wherein the number of said reconfigurable switches is at least ~~nearly~~ the same as the number of terminals of said plurality of said transistors.

15. (Original) The circuit of Claim 13 wherein said plurality of reconfigurable switches comprise reconfigurable switches having variable conductances.

16. (Currently Amended) A circuit functioning successively in two modes including a configuration mode in which the topology of said circuit is modifiable and an operation mode in which the topology of said circuit is fixed, said circuit comprising:

a plurality of transistors, each of said transistors comprising a first power terminal, a second power terminal and a control terminal, the states of said transistors changing during said operation mode;

a plurality of reconfigurable switches whose states are modifiable in accordance with an evolutionary algorithm in said configuration mode and fixed in said operating mode, each single one of said reconfigurable switches providing an individual interruptable terminal-to-terminal

PAGE 6/30 * RCVD AT 10/13/2006 1:03:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/19 * DNIS:2738300 * CSID:818 393 3160 * DURATION (mm-ss):11-28

connection between a respective pair of said transistors whereby one transistor is isolatable from another adjacent transistor, and defining an instantaneous topology of said circuit.

17. (Original) The circuit of Claim 16, wherein the number of said transistors exceeds three and the number of said reconfigurable switches is within an order of magnitude of the number of terminals of said plurality of transistors, said number of terminals including said first power terminals, said second power terminals and said control terminals of said plurality of transistors.

18. (Currently Amended) The circuit of Claim 17, wherein the number of said reconfigurable switches is ~~about~~ the same as the number of said plurality of transistors.

19. (Original) The circuit of Claim 16 wherein said plurality of reconfigurable switches comprises:

a first plurality of reconfigurable switches connected to form a first series-connected succession of said transistors, whereby each pair of successive transistors in said succession have a connection at the first power terminal of one transistor and the second power terminal of the other transistor of the pair through a corresponding single reconfigurable switch, each connection being governed by the corresponding single reconfigurable switch.

20. (Original) The circuit of Claim 16 wherein said plurality of reconfigurable switches comprises reconfigurable switches having variable conductances.

PAGE 7/30 * RCVD AT 10/13/2006 1:03:08 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-3/19 * DNIS:2738300 * CSID:818 393 3160 * DURATION (mm-ss):11-28